FORM PTO-1390 (Modified) (REV 5-93) U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTORNEY'S DOCKET NUMBER
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		016778-0445
		U S. APPLICATION NO. (If known, see 37 CFR 1.5) Unassigned 10/069222
INTERNATIONAL APPLICATION NO. PCT/JP00/05689	INTERNATIONAL FILING DATE 24 August 2000	PRIORITY DATE CLAIMED 24 August 1999

TITLE OF INVENTION
TRANSMISSION CIRCUIT

APPLICANT(S) FOR DO/EO/US
Takashi SHOJI

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   - ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   - ☒ has been transmitted by the International Bureau.
   - ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   - ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   - ☐ have been transmitted by the International Bureau.
   - ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   - ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).
11. ☐ Applicant claims small entity status under 37 CFR 1.27 .

Items 12. to 17. below concern other document(s) or information included:

12. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
13. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
14. ☐ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☒ Other items or information: Application Data Sheet (2 pages); Translation of Claim Amendments under PCT Article 34 (3 pages)

10069222 .022202

JC19 Rec'd PCT/PTO 22 FEB 2002

U.S. APPLICATION NO (If known, see 37 C.F.R. 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
Unassigned 10/069222	PCT/JP00/05689	016778-0445

18. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
Basic National Fee (37 CFR 1.492(a)(1)-(5): Search Report has been prepared by the EPO or JPO $890.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) $710.00		
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2) $740.00		
Neither international preliminary examination fee (37 CFR 1.482) nor International search fee (37 CFR 1.445(a)(2)) paid to USPTO $1,040.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) $100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$890.00	
Surcharge of $130.00 for furnishing the oath or declaration later than 20 Months from the earliest claimed priority date (37 CFR 1.492(e))		

Claims	Number Filed		Included in Basic Fee		Extra Claims		Rate		
Total Claims	2	-	20	=	0	×	$18.00	$0.00	
Independent Claims	2	-	3	=	0	×	$84.00	$0.00	
Multiple dependent claim(s) (if applicable)							$280.00		
TOTAL OF ABOVE CALCULATIONS =								$890.00	
Reduction by ½ for filing by small entity, if applicable.								$0.00	
SUBTOTAL =								$890.00	
Processing fee of $130.00 for furnishing English translation later the 20 months from the earliest claimed priority date (37 CFR 1.492(f). +									
TOTAL NATIONAL FEE =								$890.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property +								$40.00	
TOTAL FEES ENCLOSED =								$930.00	

				Amount to be: refunded	$
				charged	$

a. ☒ A check in the amount of $930.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. 19-0741 in the amount of $0.00 to the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 19-0741. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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22428

PATENT TRADEMARK OFFICE

S. G. Bent, Reg. #29,768
SIGNATURE

for NAME DAVID A. BLUMENTHAL

REGISTRATION NUMBER 26,257

DESCRIPTION

TRANSMISSION CIRCUIT

Technical Field

The present invention relates to a transmission circuit for use in CDMA communication, and, more particularly, to a transmission circuit capable of adjusting a transmission timing by a delay in CDMA mobile communication.

Background Art

In a code division multiple access (CDMA) system, a transmitter spreads an information sequence to be transmitted in the same frequency band by using different spread codes channel by channel and transmits it as a transmission signal, and a receiver receives the transmission signal as a reception signal and despreads the reception signal with the same spread code as used in transmission to acquire the information sequence.

In the most basic direct spread CDMA system, every information sequence to be transmitted in the same frequency band is spread by different spread codes and codes which have both excellent auto-correlation and cross-correlation are normally used as spread codes.

When a mobile unit moves over areas covered by a plurality of base stations in case where the CDMA system is adapted to mobile communication, a process called hand-over which switches the base station that retains the mobile unit is carried out. Hand-over in the CDMA system generally takes a scheme of receiving transmission signals from both the base station of a handing-over side and the base station of a handed-over side and sequentially shifting the reception

ratio from the base station of the handing-over side to the base station of the handed-over side, whereby hand-over without interruption of a received information sequence is executed.

By the way, a mobile unit receives a synthesized wave of a plurality of frequency- and time-multiplexed transmission signals as a reception signal, though individual spread codes are different, and acquires an information sequence addressed to itself by performing despreading with a predetermined spread code. If a reception circuit is designed to have a plurality of despreading circuits, therefore, the reception circuit can receive a plurality of information sequences.

In this case, if the transmission timing differs base station by base station, a mobile unit needs to match the timings of the transmission signals from both base stations. As a result, the amount of information to be stored increases. That is, the size of a memory or the like for storing information increases, which is inconvenient for a mobile unit that needs to be made compact. It is therefore desirable that the transmission timings of both base stations should perfectly coincide with each other.

To match the transmission timings, base stations generally transmit transmission signals at a specific timing on the absolute time using GPS and it is necessary to define the absolute time at the transmission antenna end of each base station in order to completely match the transmission timings of the individual base stations with one other.

However, not every base station can be sited under the same site conditions, and the feeder line length to the antenna from the transmission device of a base station often differs from one base station to another.

To match the heads of the periods of spread codes, the heads of the spread codes need to be adjustable to an arbitrary timing. In general, this kind of timing adjustment uses a memory, such as a FIFO memory, and spread codes for a predetermined delay are stored in the memory, after which spread signals are output from the memory. That is, a circuit, such as a FIFO memory, for sampling information for one period of a spread code with the resolution for adjustment with predetermined precision and storing it is needed.

To ensure adjustment with high precision by increasing the resolution, however, the circuit scale of a base station increases, leading to a cost increase. In case where the period of a spread code is 64 octets, for example, the capacity of a FIFO memory or the like needed increases to 256 octets from 64 octets in order to increase the resolution quadruple.

The invention aims at providing a transmission circuit for CDMA communication which can adjust the transmission timing while reducing the circuit scale.

Disclosure of Invention

The invention provides a transmission circuit for transmitting an input signal which is given a predetermined delay amount, characterized by having first delay means for giving a delay of a predetermined resolution to the input signal, second delay means for giving a higher delay than the predetermined resolution to an output signal of the first delay means, and control means for computing a first delay amount which is a maximum value that does not exceed the predetermined delay amount and can be given by a delay of the predetermined resolution, instructing the first delay means the first delay amount, computing a second delay amount which is the first delay

amount subtracted from the predetermined delay amount and instructing the second delay means the second delay amount.

Further, the invention provides a transmission circuit to be used in a mobile communications system for transmitting transmission signals from a plurality of base stations with a matched transmission timing, characterized in that each of the base stations is equipped with first delay means for giving a delay of a predetermined resolution to an input signal, second delay means for giving a delay to an output signal of the first delay means with a higher resolution than the first delay means, and control means for computing a first delay amount which is a maximum value that does not exceed a predetermined delay amount and can be given by the predetermined resolution, instructing the first delay means the first delay amount, computing a second delay amount which is the first delay amount subtracted from the predetermined delay amount and instructing the second delay means the second delay amount.

The invention also provides a transmission circuit to be used in a mobile communications system which has a plurality of base stations for synthesizing and transmitting a plurality of input signals as a transmission signal and transmits the transmission signal from each of the base stations with a matched transmission timing, characterized by having first delay means for giving a delay of a predetermined resolution to each of the input signals, synthesizing means for synthesizing a plurality of output signals output from the first delay means to acquire a synthesized signal, second delay means for giving a delay of a high resolution to the synthesized signal to acquire the transmission signal, and control means for computing a first delay amount which is a maximum value that does not exceed a predetermined delay amount and can be given by a delay with the predetermined resolution,

instructing the first delay means the first delay amount, computing a second delay amount which is the first delay amount subtracted from the predetermined delay amount and instructing the second delay means the second delay amount.

If the first and second delay means are constituted by a FIFO memory, for example, a memory with (the amount of data for an adjusting range) + (the magnification of the resolution of the second delay means with respect to the first delay means) will do in the transmission circuit of the invention whereas the conventional transmission circuit requires a memory with (the amount of data for an adjusting range) x (the magnification of the resolution of the second delay means with respect to the first delay means). That is, it is possible to realize a transmission circuit which can give a delay of a high resolution with a smaller circuit scale.

Further, if the resolution of the second delay means is set equal to the sampling period of the output signal of the transmission filter, the function of performing up-sampling can be achieved by the transmission filter that is essential in a transmitter, thus making it unnecessary to separately perform up-sampling.

Brief Description of Drawings

Fig. 1 is a block diagram showing one example of a transmission circuit for CDMA communication according to the invention.

Fig. 2 is a timing chart for explaining timing adjustment in the transmission circuit shown in Fig. 1.

Fig. 3 is a block diagram showing another example of the transmission circuit for CDMA communication according to the invention.

Best Mode for Carrying Out the Invention

The invention will now be described with reference to the drawings.

Referring to Fig. 1, information sequences S1 to Sn (n being an integer equal to or greater than 2) are information sequences to be transmitted. Spread code generating circuits 11 to 1n respectively generate spread codes to be used to spread the information sequences S1 to Sn. Multipliers 21 to 2n respectively multiply the information sequences S1 to Sn by spread codes supplied from the spread code generating circuits 11 to 1n, spread the information sequences S1 to Sn and output first to n-th spread signals.

First timing adjusting circuits 31 to 3n are controlled by a control section 80 and adjust transmission timings by respectively giving delays which are i times (hereinafter, i is called a first delay stage quantity. i is an integer equal to or greater than 1) the sampling periods of spread codes to output signals of the multipliers 21 to 2n (first to n-th spread signals). For example, the first timing adjusting circuits 31 to 3n each of which is constituted by a FIFO memory hold input signals (i.e., the first to n-th spread signals) by times to be delayed by giving a difference of an i address to a write address and a read address which are to be simultaneously accessed, and then output them.

Transmission filters 41 to 4n are transmission filters which limit the frequency components of output signals of the first timing adjusting circuits 31 to 3n (hereinafter respectively called first to n-th first timing output signals) and form transmission waves, and are oversampling filters which output signals of a shorter period (hereinafter called an oversampling period) than the sampling period of spread codes.

Second timing adjusting circuits 51 to 5n are controlled by the control section 80 and adjust transmission timings by respectively giving

delays which are j times (hereinafter, j is called a second delay stage quantity. j is an integer equal to or greater than 1) the oversampling period to output signals of the transmission filters 41 to 4n (hereinafter respectively called first to n-th filter output signals).

For example, the second timing adjusting circuits 51 to 5n each of which is constituted by a FIFO memory hold input signals by times to be delayed by giving a difference of a j address to a write address and a read address which are to be simultaneously accessed, and then output them.

A synthesizer 60, which is, for example, an adder, synthesizes output signals of the second timing adjusting circuits 51 to 5n (hereinafter respectively called first to n-th second timing output signals) to generate a transmission signal.

A transmission timing setting section 70 instructs the control section 80 a desired delay amount at its base station. The control section 80 computes the first delay stage quantity and the second delay stage quantity based on the delay amount instructed by the transmission timing setting section 70, instructs the first timing adjusting circuits 31 to 3n the first delay stage quantity and instructs the second timing adjusting circuits 51 to 5n the second delay stage quantity.

As mentioned above, as the transmission timing setting section 70 instructs a predetermined delay amount, the control section 80 computes the first delay stage quantity and the second delay stage quantity from the instructed delay amount, instructs the first timing adjusting circuits 31 to 3n the first delay stage quantity and instructs the second timing adjusting circuits 51 to 5n the second delay stage quantity.

Meanwhile, the information sequences S1 to Sn are multiplied by the spread codes generated by the spread code generating circuits 11

to 1n and spread by the multipliers 21 to 2n to become the first to n-th spread signals. Then, the first to n-th spread signals are given to the first timing adjusting circuits 31 to 3n.

The first timing adjusting circuits 31 to 3n respectively delay the first to n-th spread signals by giving a difference of the first delay stage quantity instructed by the control section 80 to the write address and read address which simultaneously access the FIFO memories, and output the first to n-th first timing output signals. Then, the first to n-th first timing output signals are respectively input to the transmission filters 41 to 4n. The transmission filters 41 to 4n respectively limit the frequencies of the first to n-th first timing output signals, perform up-sampling by interpolating the sampling period and output the first to n-th filter output signals to the second timing adjusting circuits 51 to 5n.

The second timing adjusting circuits 51 to 5n respectively delay the first to n-th filter output signals by giving a difference of the second delay stage quantity instructed by the control section 80 to the write address and read address which simultaneously access the FIFO memories, and output the first to n-th second timing output signals. Then, the first to n-th second timing output signals are synthesized by the adder 60 to be a transmission signal.

Here, referring also to Fig. 2, the resolution of the second timing adjusting circuits 51 to 5n is, for example, four times the resolution of the first timing adjusting circuits 31 to 3n. That is, a case where the transmission filters 41 to 4n perform quadruple up-sampling is illustrated. The period of the spread codes is 64 octets. The predetermined delay amount is, for example, six stages in terms of the resolution of the second timing adjusting circuits 51 to 5n.

As mentioned above, the control section 80 which has been instructed the predetermined delay amount by the transmission timing

setting section 70 instructs the first delay stage quantity i = 1 the first timing adjusting circuits 31 to 3n and instructs the second delay stage quantity j = 2 the second timing adjusting circuits 51 to 5n.

The first to n-th spread signals which are respectively output from the multipliers 21 to 2n are first subjected to a delay of a first stage by the first timing adjusting circuits 31 to 3n, then are up-sampled by the transmission filters 41 to 4n and are further subjected to a delay of a second stage by the second timing adjusting circuits 51 to 5n.

As timing adjustment is carried out by two kinds of timing adjusting circuits of different resolutions as described above, the required capacity of the FIFO memory can be small and high-resolution timing adjustment can be carried out.

In case where the period of the spread codes is 64 octets, a memory capacity of 256 (64 x 4) octets was needed conventionally in order to ensure a structure which can execute timing adjustment with a quadruple resolution, whereas a memory capacity of 68 (64 + 4) octets will do in the above-described example. That is, even if high-resolution timing adjustment is performed, an increase in circuit scale is suppressed and a transmission circuit at a low cost can be realized at a low cost.

Note that the transmission circuit is used in, for example, a base station of a CDMA mobile communications system. In this case, a base station which is able to carry out high-resolution timing adjustment can be constructed at a low cost, and, what is more, the transmission timings can be matched accurately among base stations even if the site conditions for the base stations are different. This results in an increased degree of freedom of the site conditions for base stations. That is, the transmission timing of every base station can be adjusted at the antenna end without increasing the cost of the base station. As a

result, timing adjustment in a mobile unit becomes unnecessary, so that the cost of the CDMA mobile communications system can be reduced.

Referring to Fig. 3, another example of the transmission circuit according to the invention will be explained.

The illustrated transmission circuit has a timing adjusting circuit (hereinafter called a third timing adjusting circuit) which performs a delay by k times the oversampling period (hereinafter k is called a third delay stage quantity. k is an integer equal to or greater than 1) in place of the second timing adjusting circuits 51 to 5n of the transmission circuit shown in Fig. 1, and this third timing adjusting circuit 90 is located at the subsequent stage of an adder 61. As the other structure is the same as that of the example shown in Fig. 1, its description will be omitted.

In the transmission circuit shown in Fig. 3, the control section 80 computes a first delay stage quantity and a third delay stage quantity from a delay amount instructed by the transmission timing setting section 70. Then, the control section 80 instructs the first timing adjusting circuits 31 to 3n the first delay stage quantity and instructs the third timing adjusting circuit 90 the third delay stage quantity.

As has been described in conjunction with Fig. 1, the first to n-th filter output signals are synthesized (the output signal of the adder 61 is called a synthesized signal in Fig. 3). The synthesized signal is input to the third timing adjusting circuit 90. The third timing adjusting circuit 90 gives a difference of the third delay stage quantity instructed by the control section 80 to the write address and read address which are to be simultaneously accessed to delay the synthesized signal, and outputs it as a transmission signal.

In the example shown in Fig. 3, as described above, the synthesized signal is delayed by k times the oversampling period by the

third timing adjusting circuit, so that high-resolution timing adjustment can be carried out while further reducing the required capacity of the FIFO memory, i.e., suppressing an increase in circuit scale, and also reducing the cost.

Although the descriptions of the examples shown in Figs. 1 and 3 have been given of a case where the first timing adjusting circuits, the second timing adjusting circuits and the third timing adjusting circuit 90 are constituted by memories, the first timing adjusting circuits, the second timing adjusting circuits and the third timing adjusting circuit 90 may be constituted by shift registers.

Industrial Applicability

As described above, the invention can give a delay with a high resolution while reducing the circuit scale, so that high-resolution transmission timing adjustment can be carried out a low cost in, for example, CDMA mobile communication.

Amended Claims

1. (Deleted)
2. (Deleted)
3. (Deleted)
4. (Deleted)
5. (Amended) A transmission circuit to be used in a mobile communications system for transmitting transmission signals from a plurality of base stations with a matched transmission timing, each of said base stations being equipped with first delay means for giving a delay of a predetermined resolution to an input signal, comprising:

second delay means for giving a delay to an output signal of said first delay means with a higher resolution than said first delay means,

control means for computing a first delay amount which is a maximum value that does not exceed a predetermined delay amount and can be given by said predetermined resolution, instructing said first delay means said first delay amount, computing a second delay amount which is said first delay amount subtracted from said predetermined delay amount and instructing said second delay means said second delay amount,

transmission timing setting means for notifying said control means of said predetermined delay amount as a transmission timing, and

a transmission filter constituted by an oversampling filter being provided between said first delay means and said second delay means, wherein:

said resolution of said second delay means is equal to a sampling period of an output signal of said transmission filter.

6. (Deleted)

7. (Deleted)

8. (Deleted)

9. (Amended) A transmission circuit to be used in a mobile communications system which has a plurality of base stations for synthesizing and transmitting a plurality of input signals as a transmission signal and transmits said transmission signal from each of said base stations with a matched transmission timing, said input signal being a spread signal obtained by spreading an information sequence based on a spread code, comprising:

first delay means for giving a delay of a predetermined resolution to each of said input signals,

synthesizing means for synthesizing a plurality of output signals output from said first delay means to acquire a synthesized signal,

second delay means for giving a delay of a high resolution to said synthesized signal to acquire said transmission signal,

control means for computing a first delay amount which is a maximum value that does not exceed a predetermined delay amount and can be given by a delay with said predetermined resolution, instructing said first delay means said first delay amount, computing a second delay amount which is said first delay amount subtracted from said predetermined delay amount and instructing said second delay means said second delay amount,

transmission timing setting means for notifying said control means of said predetermined delay amount as a transmission timing, and

a transmission filter constituted by an oversampling filter being provided between said first delay means and said synthesizing means, wherein:

said resolution of said second delay means is equal to a sampling period of an output signal of said transmission filter.

10. (Deleted)

11. (Deleted)

12. (Deleted)

Abstract

This transmission circuit is used in, for example, a base station in CDMA mobile communication. The transmission circuit has a first delay circuit section which gives a delay to an input signal (spread signal) with a predetermined resolution, and a second delay circuit section gives a delay to the output signal of the first delay circuit section with a higher resolution than the predetermined resolution. A control section computes a first delay amount which is a maximum value that does not exceed a predetermined delay amount and can be given by a delay of the predetermined resolution, instructs the first delay circuit section the first delay amount, computes a second delay amount which is the first delay amount subtracted from the predetermined delay amount and instructs the second delay circuit section the second delay amount. By adjusting a transmission timing this way, it is possible to adjust the transmission timing among a plurality of base stations while reducing the circuit scale.

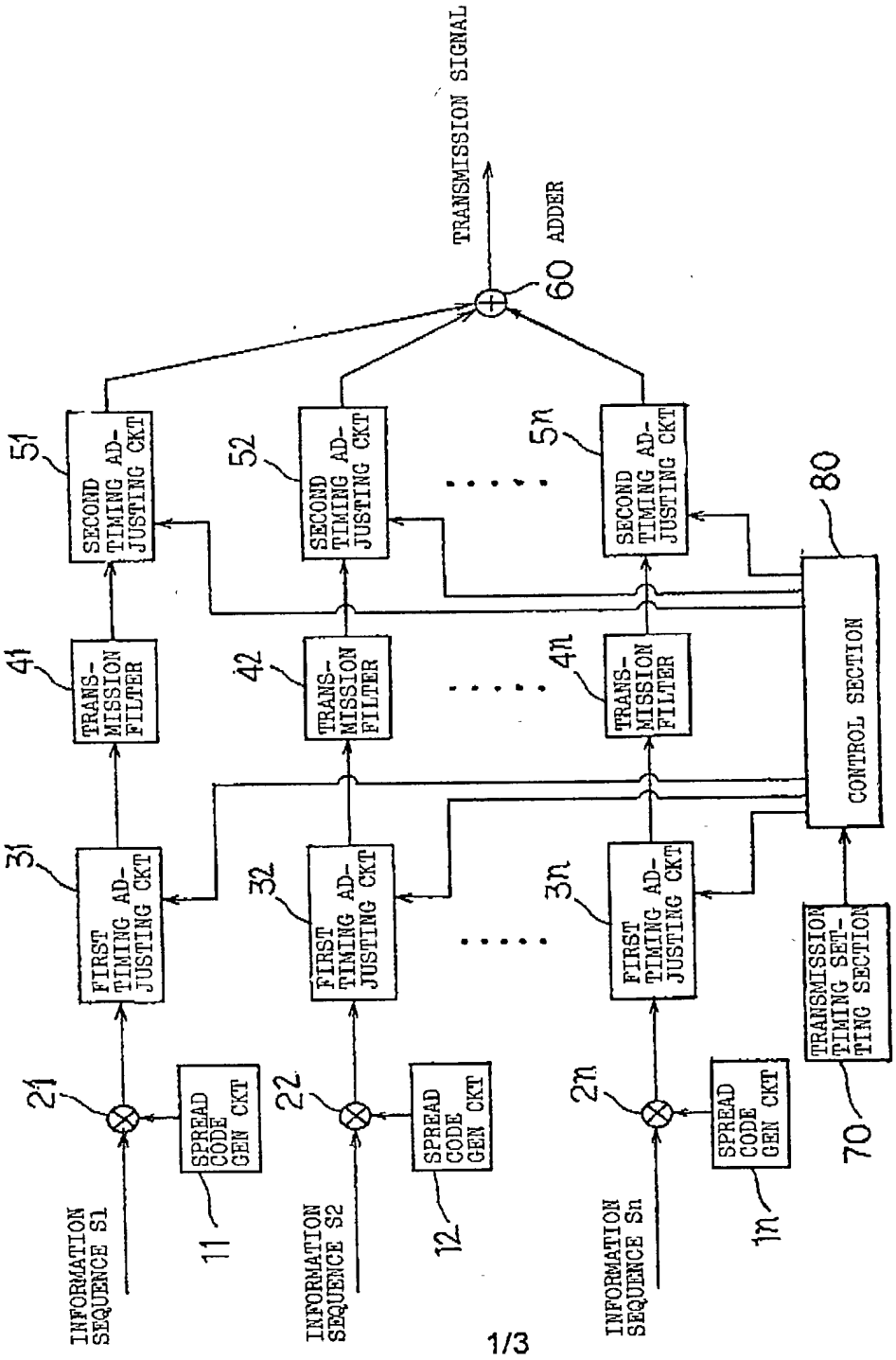

TRANSMISSION SIGNAL
60 ADDER
51
SECOND TIMING ADJUSTING CKT
52
SECOND TIMING ADJUSTING CKT
5n
SECOND TIMING ADJUSTING CKT
80
CONTROL SECTION
41
TRANSMISSION FILTER
42
TRANSMISSION FILTER
4n
TRANSMISSION FILTER
31
FIRST TIMING ADJUSTING CKT
32
FIRST TIMING ADJUSTING CKT
3n
FIRST TIMING ADJUSTING CKT
TRANSMISSION TIMING SETTING SECTION
70
21
22
2n
SPREAD CODE GEN CKT
SPREAD CODE GEN CKT
SPREAD CODE GEN CKT
11
12
1n
INFORMATION SEQUENCE S1
INFORMATION SEQUENCE S2
INFORMATION SEQUENCE Sn

FIG. 1

Title: TRANSMISSION CIRCUIT
Inventor(s): Takashi SHOJI
Atty. Docket No.: 016778-0445

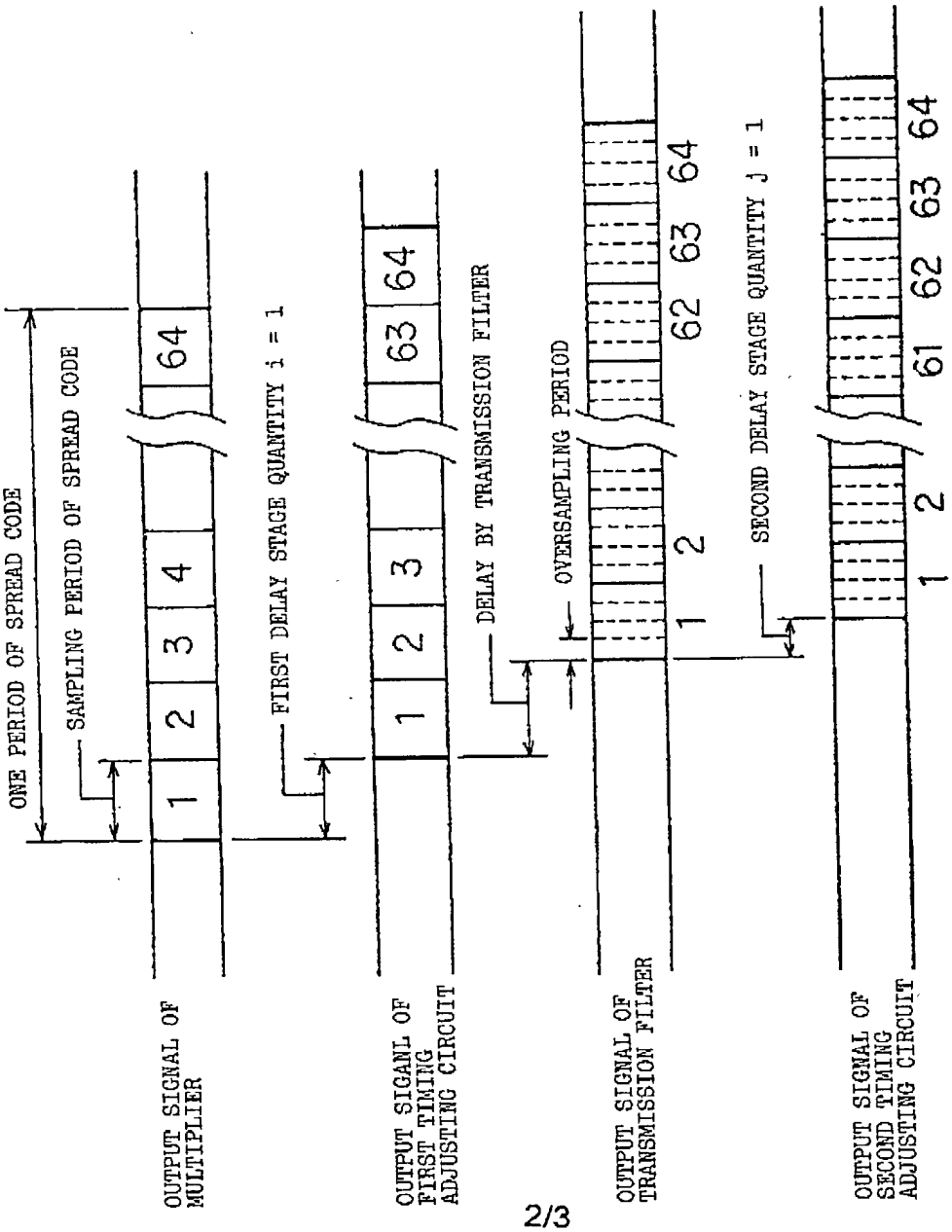
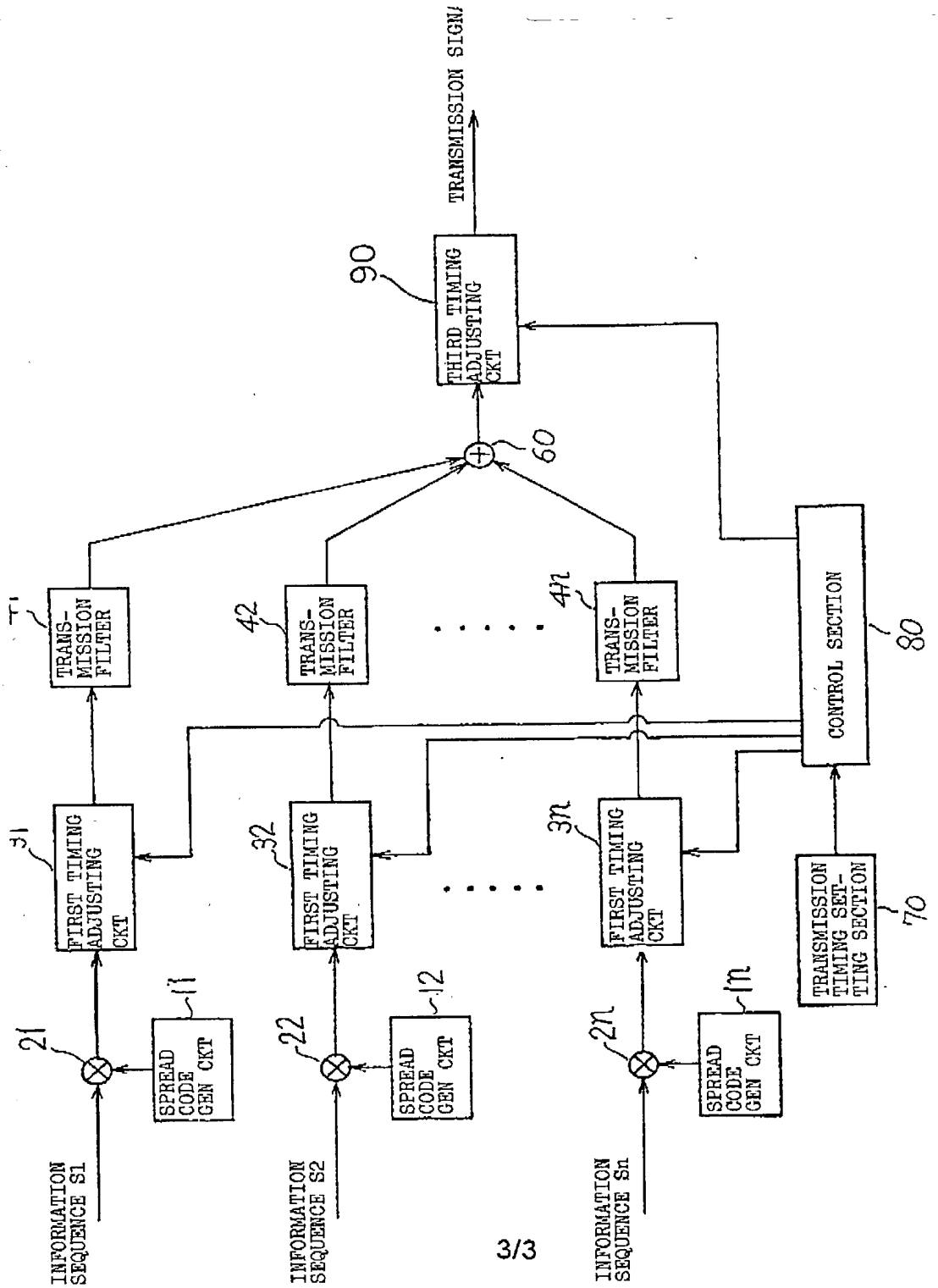


FIG. 2


TRANSMISSION SIGNAL
90
THIRD TIMING ADJUSTING CKT
60
TRANS-MISSION FILTER
41
42
4n
CONTROL SECTION
80
31
32
3n
FIRST TIMING ADJUSTING CKT
TRANSMISSION TIMING SETTING SECTION
70
11
12
1n
SPREAD CODE GEN CKT
21
22
2n
INFORMATION SEQUENCE S1
INFORMATION SEQUENCE S2
INFORMATION SEQUENCE Sn

533-10317
WN-2223 (P)

Attorney Docket No. _____

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I HEREBY DECLARE:

THAT my residence, post office address, and citizenship are as stated below next to my name;

THAT I believe I am the original, first, and sole inventor (if only one inventor is named below) or an original, first, and joint inventor (if plural inventors are named below or in an attached Declaration) of the subject matter which is claimed and for which a patent is sought on the invention entitled

TRANSMISSION CIRCUIT

the specification of which (check one)

____ is attached hereto.

__x__ was filed on 8/24/2000 as United States Application Number or PCT International Application Number PCT/JP00/05689 and was amended on 4/27/2001 (if applicable).

THAT I do not know and do not believe that the same invention was ever known or used by others in the United States of America, or was patented or described in any printed publication in any country, before I (we) invented it;

THAT I do not know and do not believe that the same invention was patented or described in any printed publication in any country, or in public use or on sale in the United States of America, for more than one year prior to the filing date of this United States application;

THAT I do not know and do not believe that the same invention was first patented or made the subject of an inventor's certificate that issued in any country foreign to the United States of America before the filing date of this United States application if the foreign application was filed by me (us), or by my (our) legal representatives or assigns, more than twelve months (six months for design patents) prior to the filing date of this United States application;

THAT I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment specifically referred to above;

THAT I believe that the above-identified specification contains a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is

Attorney Docket No. _____

most nearly connected, to make and use the invention, and sets forth the best mode contemplated by me of carrying out the invention; and

THAT I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I HEREBY CLAIM foreign priority benefits under Title 35, United States Code §119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number	Country	Foreign Filing Date	Priority Claimed?	Certified Copy Attached?
11-236946	Japan	August 24, 1999	yes	

I HEREBY CLAIM the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below.

U.S. Provisional Application Number	Filing Date

I HEREBY CLAIM the benefit under Title 35, United States Code, §120 of any United States application(s), or § 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Attorney Docket No. _____

U.S. Parent Application Number	PCT Parent Application Number	Parent Filing Date	Parent Patent Number

I HEREBY APPOINT the following registered attorneys and agents of the law firm of FOLEY & LARDNER to have full power to prosecute this application and any continuations, divisions, reissues, and reexaminations thereof, to receive the patent, and to transact all business in the United States Patent and Trademark Office connected therewith:

STEPHEN A. BENT	Reg. No. 29,768
DAVID A. BLUMENTHAL	Reg. No. 26,257
BETH A. BURROUS	Reg. No. 35,087
ALAN I. CANTOR	Reg. No. 28,163
WILLIAM T. ELLIS	Reg. No. 26,874
JOHN J. FELDHAUS	Reg. No. 28,822
PATRICIA D. GRANADOS	Reg. No. 33,683
JOHN P. ISACSON	Reg. No. 33,715
MICHAEL D. KAMINSKI	Reg. No. 32,904
LYLE K. KIMMS	Reg. No. 34,079
KENNETH E. KROSIN	Reg. No. 25,735
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GLENN LAW	Reg. No. 34,371
PETER G. MACK	Reg. No. 26,001
BRIAN J. MC NAMARA	Reg. No. 32,789
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RICHARD C. PEET	Reg. No. 35,792
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BERNHARD D. SAXE	Reg. No. 28,665
CHARLES F. SCHILL	Reg. No. 27,390
RICHARD L. SCHWAAB	Reg. No. 25,479
ARTHUR SCHWARTZ	Reg. No. 22,115
HAROLD C. WEGNER	Reg. No. 25,258

and I request that all correspondence be directed to:

David A. Blumenthal
FOLEY & LARDNER
3000 K Street, N.W., Suite 500
Washington, D.C. 20007-5109

Telephone: 202-672-5407
Facsimile: 202-672-5399

I UNDERSTAND AND AGREE THAT the foregoing attorneys and agents appointed by me to prosecute this application do not personally represent me or my legal interests, but instead represent the interests of the legal owner(s) of the invention described in this application.

Attorney Docket No. _____

I FURTHER DECLARE THAT all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Name of first inventor	TAKASHI SHOJI
Residence	Tokyo, Japan JPX
Citizenship	Japanese
Post Office Address	c/o NEC Corporation, 7-1, Shiba 5-chome, Minato-ku, Tokyo, Japan
Inventor's signature	Takashi Shoji
Date	February 21, 2002
Name of second inventor	
Residence	
Citizenship	
Post Office Address	
Inventor's signature	
Date	
Name of third inventor	
Residence	
Citizenship	
Post Office Address	
Inventor's signature	
Date	